Vin Shin

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Education

University of California, Santa Barbara – B.S. in Electrical & Computer Engineering — Expected June 2028

- **GPA:** 3.76/4.00 **Awards:** Dean's Honors
- **Relevant Coursework:** Semiconductor Devices, Digital Design Principles (Verilog, FPGA), Continuous & Discrete Signal analysis, Foundational Circuits

Experience

Electrical Technical Director – UCSB Gaucho Racing (FSAE Electric, GR27) — June 2026 – Present

- Lead 23-person electrical team across 4 subteams (Electronic Controls, Driverless, LV Power & Harness, Powertrain Electronics); authored department-wide restructuring proposal establishing
- Own system-level architecture: power budget, CAN DBC, shutdown circuit state machine, and driverless system conversion (EBS, DSMS, DSSI, SDC modifications) for FSAE EV + DV rules compliance.
- Single point of technical authority for all electrical design reviews, cross-team interface disputes, and integration testing across subteam boundaries.

Low Voltage Electronics Lead – UCSB Gaucho Racing (GR26) — June 2025 – June 2026

- Led LV electrical subsystem design for GR26: GLV battery, DC-DC power distribution, wire harness, driver interface, and sensor integration.
- Reduced full-vehicle connector count 60% (52 $\rightarrow$ 21) through consolidated harness architecture, improving serviceability and reducing potential failure points.
- Delivered CAN-based driver interface PCB (STM32 + WS2812b dashboard) and IP-rated attic enclosure housing primary power distribution.
- Coordinated cross-functional integration with HV, mechanical, and firmware teams to meet FSAE competition deadlines and rules compliance.

Projects

Mako Shortfin — 1.5 kW Field-Oriented BLDC Motor Controller — 2025 – 2026

- Designed and brought up 1.5 kW FOC inverter: 30 kHz switching, 25 A peak AC, 60 V DC bus, Infineon OptiMOS MOSFETs driven by UCC27211A half-bridge drivers; achieved closed-loop current + velocity control.
- 4-layer mixed-signal PCB with 2 oz inner-layer copper, cascaded buck-converter bias rails, and isolated analog/digital returns for low-noise current sensing.
- STM32G474 firmware implementing synchronized 3-phase inline current sampling, and A1333 SPI magnetic encoder feedback in a 30 kHz Field-Oriented control loop.

2.4 GHz LNA Design – RF Analog Project (ADS) — 2025 – 2026

- Designed 2.4 GHz low-noise amplifier in Keysight ADS using Infineon BFP740F SiGe HBT (V_{CE} = 3 V, I_C = 15 mA); achieved $\sim$18 dB gain and NF $\sim$1.84 dB.
- Performed full S-parameter analysis, K-factor stability check, simultaneous noise/input matching via Smith-chart-based L-network synthesis, and conditional stability mitigation.

GR26 Battery Management System – UCSB Gaucho Racing — Sept. 2025

- Designed schematic and 4-layer PCB for GR26 segment-level BMS modules using NXP MC33771C AFE in 2p140s configuration; 39% board area reduction vs. GR25 improved pack packaging density and thermal margin.
- Implemented STM32G474 thermistor acquisition for 14 temperature points per segment with 10-sample moving-average filter achieving $<$0.5°C noise floor.
- Integrated TPL (Transformer Physical Layer) daisy-chain across 10 modules with capacitive isolation for cell monitoring and passive balancing.

GR26 Wire Harness Architecture – UCSB Gaucho Racing — Dec. 2025

- Developed full-vehicle electrical schematic in RapidHarness mapping power, CAN, and analog signal paths across 8 subsystems; exported wire-level documentation for fabrication.

- Routed harness in SolidWorks Routing maintaining FSAE clearance requirements through monocoque while optimizing serviceability for pit-lane replacement.
- Specified shielded twisted-pair CAN, DR25 heat-shrink covering, and Deutsch motorsport connectors for EMI-resilient interconnect under vibration.

Technical Skills

Languages: C/C++, Python, MATLAB, Verilog/SystemVerilog, STM32 HAL/LL

EDA Tools: Altium Designer, KiCad, LTspice, Keysight ADS, Fusion 360, SolidWorks, RapidHarness

Domains: Power electronics, embedded systems (STM32, CAN/SPI/I^2C/UART), mixed-signal PCB design (multilayer, SI/PI, EMI mitigation), FPGA (Verilog, digital synchronous design), BMS, wire harness engineering

Bench: Oscilloscope, logic analyzer, soldering (SMD/THT rework), thermal imaging, power supply + electronic load characterization

Standards / Frameworks: FSAE EV + DV rules, IPC-2221/2222 PCB design, basic UL/IEC safety awareness for HV systems